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EXAMINER	
JELINEK, BRIAN J	

ART UNIT	PAPER NUMBER
2622	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/824,007	SUZUKI, NOBUO	
	Examiner	Art Unit	
	Brian Jelinek	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-8 and 10-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-8 and 10-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 April 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Amendment

The Examiner respectfully submits a response to the amendment received on 1/6/2006 of application no. 09/824,007 filed on 4/3/2001 in which claims 1, 4-8, and 10-20 are currently pending.

Arguments

The Applicant's arguments have been fully considered but they are not persuasive. Please refer to the following office action, which clearly sets forth the reasons for non-persuasiveness.

The Applicant argues:

> Applicant's independent claims 1 and 14 each include the limitation of "a reset transistor connected between said cathode and said power source line, and having a gate connected to an associated reset signal line." In the Office Action, the Examiner asserts that Roberts discloses a reset transistor 70 connected between the cathode and the power source line, and having a gate 68 connected to an associated reset signal line. See, e.g., Office Action, Page 3, Lines 14-16. Applicants respectfully disagree with the Examiner's assertions. For example, in Roberts, the gate of FET 70 is connected to the output of a NOR gate 64. See, e.g., Roberts, Column 5, Lines 44-46, and Figure 2. As such, the gate of FET 70 is not connected to a reset signal line. Consequently, FET 70 cannot correspond to Applicant's claimed reset transistor, as set forth in independent claims 1 and 14.

In response, an input connected to the gate of a reset transistor for controlling said transistor is, by definition, a reset signal line.

The Applicant further argues:

> New independent claim 20 claims a row-by-row nature of an image pickup device. In contrast, Roberts is based on a completely different random access design, and is not compatible with the row-by-row features of independent claim 20.

In response, the random access image pickup device of Roberts is compatible with the conventional row-by-row imaging device, the image pickup device of Roberts being a more general implementation of the conventional row sequential image pickup device because the image pickup device of Roberts can perform row-by-row output in addition to allowing random access on a pixel-by-pixel basis. In particular, reset transistor 70 of a particular pixel may be reset by simultaneous selection of address lines 56 and 58, thereby applying a reset signal to the gate of the reset transistor 70. Clearly, any given row of pixels can be reset by the application of all column address lines simultaneously with the corresponding row address line.

Claim Objections

The numbering of claims is not in accordance with 37 CFR 1.126 which requires the original numbering of the claims to be preserved throughout the prosecution. When claims are canceled, the remaining claims must not be renumbered. When new claims are presented, they must be numbered consecutively beginning with the number next following the highest numbered claims previously presented (whether entered or not).

Misnumbered claim 1 (2^{nd} occurrence) has been renumbered as claim 20.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 4-8, 10-13, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Roberts (U.S. Pat. No. 5,452,004):

Regarding claim 1, Roberts discloses a MOS-type solid-state image pickup device, comprising: a semiconductor substrate (Fig. 1, element 14); a large number of pixels arranged in one surface of the semiconductor substrate in an array having a plurality of rows and a plurality of columns (Fig. 1, element 12), each pixel (Fig. 1, element 40) including (a) a photoelectric converter element having a cathode (Fig. 9, element 42) and (b) a switching circuit (Fig. 9, element 40) electrically connected to the photoelectric converter element for controlling generation of an output signal representing electric charge accumulated in the photoelectric converter element and discharge of the electric charge (col. 8, line 44-55); a plurality of row selection signal lines (Fig. 2, element 56) disposed along a row direction, each being associated with one pixel row for supplying a row selection signal; a plurality of output signal lines (Fig. 9, CCVL) disposed along a column, each being associated with at least one pixel column; a plurality of reset signal lines (Fig. 2, element 68) disposed along the row direction, each being associated with one pixel row for supplying a reset signal (col. 8,

lines 44-55; col. 7, lines 11-26); a power source line (Fig. 2, element Vssa); and an overall reset controller (Fig. 1, element 208; col. 12, lines 28-50) supplying an overall reset signal to all of said reset signal lines at a time; wherein said switching circuit comprises: a series connection of an output transistor (Fig. 2, element 74) and a selection transistor (Fig. 2, element 76) connected between the power source line and an associated output signal line, the output transistor having a gate being capable of receiving a potential generated by the charge accumulated in said cathode (Fig. 2, element 72), the selection transistor having a gate connected to an associated row selection signal line (Fig. 2, element 80); and a reset transistor connected between said cathode and said power source line (Fig. 2, element 70); and having a gate connected to an associated reset signal line (Fig. 2, element 68).

The Examiner acknowledges that the photoconverting element 42 in Fig. 2 of Roberts has an opposite orientation as the photoconvering element 20 in Fig. 10 of the instant application. The Examiner notes that while the polarity of the charge in the circuits of Fig. 2 of Roberts and Fig. 10 of the instant application are opposite, the operation of the circuits are the same, i.e. the polarity of the charge is irrelevant to the function and effects of the circuits.

Regarding claim 4, Roberts teaches a readout row-shifter (Fig. 4, element 102) for sequentially supplying the row selection signal to the row selection signal lines; a reset row-shifter (Fig. 4, element 100) for sequentially supplying the reset signal to the reset signal lines; and an image signal outputting device electrically connected to the

output signal lines for generating an image signal representing the output signal and for sequentially outputting the image signal (col. 9, lines 1-7).

Regarding claim 5, Roberts teaches at least one analog signal generator for converting the output signal generated on each output signal line (Fig. 9, CCVL) into an analog voltage signal (Fig. 6, Vout; col. 9, lines 1-17); and a row-directional shifter for controlling operation of the analog signal generator and for sequentially outputting the analog voltage signal from the at least one analog signal generator (col. 1, lines 15-20 and 62-65).

Regarding claim 6, Roberts teaches an analog signal generator for converting the output signal generated on each output signal line into an analog voltage signal (col. 9, lines 1-17); and an analog-to-digital converter (Fig. 6, element 166) for receiving the analog voltage signal and for converting the analog voltage signal into a digital signal; and a buffer memory for receiving the digital signal, temporarily keeping the digital signal therein, and outputting the digital signal therefrom because a buffer is inherent in an A/D converter since the result is latched and held for a time in order to provide an output value.

Regarding claim 7, Roberts teaches a controller (Fig. 1, element 208) for controlling operations (col. 13, lines 22-44) of the overall reset controller, the readout row-shifter, the reset row-shifter, and the image signal outputting device.

Regarding claim 8, Roberts teaches a transfer signal line (Fig. 2, element 48) disposed for each pixel row; and a transfer control row-shifter for sequentially supplying (col. 5, line 6-13; col. 1, lines 62-65) a transfer control signal to the transfer signal lines,

and each switching circuit further comprises a transfer transistor (Fig. 2, element 46) electrically connected between said cathode and gate of the photoelectric converter element and the gate of the output transistor, which gate is also connected to the reset transistor, the transfer transistor including a control terminal electrically connected to the transfer signal line.

Regarding claim 10, Roberts discloses a readout row-shifter for sequentially supplying the row selection signal to said row selection signal lines (Fig. 3, element 114 row select); a reset row-shifter for sequentially supplying the reset signal to said reset signal lines (Fig. 3, element 112 row reset); and an image signal outputting device electrically connected to said output signal lines for generating an image signal representing the output signal and for sequentially outputting the image signal (Fig. 4, element 128, Fig. 6).

Regarding claim 11, please see the rejection of claim 5.

Regarding claim 12, please see the rejection of claim 6.

Regarding claim 13, please see the rejection of claim 7.

Regarding claim 20, please see the rejection of claim 1.

Claims 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Roberts (U.S. Pat. No. 5,452,004) in view of Ernest et al. (U.S. Pat. No. 4, 827,348).

Regarding claim 14, please see the rejections of claims 1 and 4. Furthermore, Roberts teaches the use of an additional transistor (Fig. 9, element 200) in an alternative embodiment that enables a global reset and "snap shot" capability (col. 12,

lines 28-38). One of ordinary skill in the art would have provided the additional transistor of Roberts alternative embodiment for the purpose of enabling still capture in addition to motion video capture. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to have provided the additional transistor of Roberts alternative embodiment for the purpose of enabling still capture in addition to motion video capture. Further still, Roberts teaches a still picture indication signal generator for generating a still picture indication signal indicating shooting of a still picture (col. 12, lines 28-38) because a still picture indication signal is inherent in taking a snapshot.

Although Roberts teaches the use of an electronic shutter (col. 12, lines 46-50), Roberts does not disclose a light shielding device capable of interrupting light incident to the image pickup device for a predetermined period of time after an overall reset operation. However, Ernest et al. teaches a mechanical shutter for interrupting light incident to an image pickup device (Fig. 3, element 24; col. 4, lines 11-15), which remains closed for a predetermined period of time until the still image is read out following an overall reset (Fig. 2). One of ordinary skill in the art would have provided the mechanical shutter of Ernest et al. for exposure control in a dual mode camera in order to permit high shutter speed in the still mode and electronic shuttering in the video mode (col. 3, lines 7-13). As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to provide the mechanical shutter of Ernest for exposure control in a dual mode camera in order to permit high shutter speed in the still mode and electronic shuttering in the video mode.

Furthermore, Ernest discloses a mobile picture mode controller (Fig. 3, element 20) electrically connected to said MOS-type solid-state image pickup device for continually control operation thereof for repeatedly conducting (a) an image readout operation in which the row selection signal is sequentially supplied from said readout row-shifter to a predetermined number of row selection signal lines for sequentially outputting from said image signal outputting device an image signal representing the output signal generated on each said output signal line (Fig. 3, Camera Timing and Control 20, CCD 12) because this is an inherent feature in a conventional CCD and (b) an electronic shutter operation (col. 2, lines 20-33) in which the reset signal is sequentially supplied from said reset row-shifter to said reset signal supply lines at least associated with said pixel row as an object of the image signal readout operation for sequentially discharge electric charge accumulated in said photoelectric converter elements (Fig. 3, Camera Timing and Control 20, CCD 12) because this is an inherent feature in a conventional CCD; and a first still picture mode controller (Fig. 3, element 20; Fig. 2, Still Switch On) electrically connected to said MOS-type solid-state image pickup device for controlling in place of said mobile mode controller, when the still picture indication signal is outputted, operations of said MOS-type solid-state image pickup device and said light shielding device, for conducting an overall reset operation in which the overall reset controller is operated, in a state in which the operations of said readout row-shifter and said rest row-shifter are stopped, and electric charge accumulated in all said photoelectric converter elements is discharged, and for conducting an image signal readout operation in which said light shielding device is

operated and interrupts the incident light for a predetermined period of time after the overall reset operation is finished, and the row selection signal is sequentially supplied from said readout row-shifter to said row selection signal lines for sequentially outputting an image signal representing the output signal generated on said output signal lines from said image signal outputting device (Fig. 2, Still; col. 5, line 63-col. 6, line 48).

Regarding claim 15, Ernest teaches when in the video mode (corresponding to an electronic shutter operation), and the still picture indication signal is outputted, the still picture mode controller does not interrupt the operation (Fig. 2, Still Switch On, Video, Still); when an electronic shutter operation is being executed at a point of time when the still picture indication signal is outputted, the still picture mode controller conducts once the image signal readout operation once after the electronic shutter operation (Fig. 2, Still Switch On, Video, Still); and then the first still picture mode controller conducts the overall reset operation (col. 6, lines 28-59) when a global reset is operated in preparation for a second still picture.

Regarding claim 16, please see the rejection of claim 8. Furthermore, Roberts teaches a mobile picture mode controller (Fig. 1, element 208) or the first still picture mode controller conducting the transfer control row-shifter for sequentially supplying, in the image readout operation, the row reset operation, or the overall reset operation, the transfer control signal to each transfer signal lines associated with the pixel row as an object of the operation.

Claims 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Roberts (U.S. Pat. No. 5,452,004), in view of Ernest et al. (U.S. Pat. No. 4, 827, 348), and further in view of Soeda et al. (U.S. Pat. No. 5,382,974).

Regarding claim 17, Roberts teaches motion video and still image capture (col. 1, line 55-col. 2, line 5; col. 12, lines 28-38). Furthermore, Ernest teaches a shutter that interrupts light for a predetermined period of time (please see the rejection of claim 14). Neither Roberts nor Ernest teaches the use of a strobe device or a controller for a second still picture mode comprising a strobe device.

However, Soeda et al. teaches a strobe device (Fig. 1, element 20) for emitting flash light when a predetermined signal is received (Fig. 5) or the strobe device installing device for installing therein; a second still picture mode controller (strobe mode: col. 13, lines 27-31; Fig. 3, elements S8 and S18) electrically connected to the image pickup device for controlling in place of a mobile mode controller, when the still picture indication signal is outputted; a strobe device operation signal is generated for operating the strobe device (Fig. 5); a shutter is operated for a predetermined period of time after strobe device operation signal is generated (Fig. 5); and a still picture mode specifying device (Fig. 3, element S8; col. 14, lines 24-38) for specifying a still picture mode controller to be operated when the still picture indication signal is outputted.

One of ordinary skill in the art would have provided the strobe of Soeda et al. with the imager of Roberts and Ernest et al. for the purpose of increasing the maximum photographable distance to an object and to obtain a high quality image (col. 13, line 65-col. 14, line 3). As a result, it would have been obvious to one of ordinary skill in the

art at the time of the invention to provide the strobe of Soeda et al. with the imager of Roberts and Ernest et al. for the purpose of increasing the maximum photographable distance to an object and to obtain a high quality image (col. 13, line 65-col. 14, line 3).

Regarding claim 18, Roberts teaches motion video and still image capture (col. 1, line 55-col. 2, line 5; col. 12, lines 28-38). Roberts does not specifically teach that a still picture mode does not interrupt a video mode when a still picture mode is indicated. However, Ernest et al. teaches an electronic shutter operation or an image signal readout operation is being executed at a point of time when the still picture indication signal is outputted, a still picture mode controller does not interrupt the operation; and when an electronic shutter operation is being executed at a point of time when the still picture indication signal is outputted, a still picture mode controller conducts the image signal readout operation once after the electronic shutter operation; and then a still picture mode controller conducts the overall reset operation (Fig. 2, Clear CCD; col. 5, line 63-col. 6, line 48).

Regarding claim 19, please see the rejection for the rejection of claim 16.

Prior Art Made of Record

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Matsunaga et al. (U.S. Pat. No. 6,239,839) discloses a conventional three transistor pixel cell (Fig. 1).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian Jelinek whose telephone number is (571) 272-7366. The examiner can normally be reached on M-F 9:00 am - 5:00 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ngoc-Yen Vu can be reached at (571) 272-7320. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brian Jelinek
3/17/2006

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SUPERVISORY PATENT EXAMINER